PCM4222EVM User's Guide

This document serves as a reference for the PCM4222EVM evaluation module. When used in conjunction with commonly available audio test equipment, the PCM4222EVM provides a complete environment for evaluating the functionality and performance of the PCM4222 integrated circuit. Indirectly, the PCM4222EVM serves as an evaluation platform for the PCM4220 integrated circuit; the PCM4220 is a subset derivative of the PCM4222 device.

This document includes information regarding absolute operating conditions, power-supply requirements, and hardware configuration for the evaluation module. The electrical schematics and bill of materials are also included for reference purposes. Throughout this document, the acronym *EVM* and the phrase *evaluation module* are synonymous with the PCM4222EVM.

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1 Introduction

The PCM4222EVM evaluation module from Texas Instruments provides a convenient platform for testing the PCM4222, a high-performance, stereo audio analog-to-digital (A/D) converter integrated circuit. Figure 1 shows a block diagram of the PCM4222 device. Refer to the PCM4222 product datasheet for additional information and details regarding this product. The PCM4222EVM evaluation module includes analog input and digital output circuitry with common audio connectors, providing a direct interface to audio test systems for measurement and evaluation.

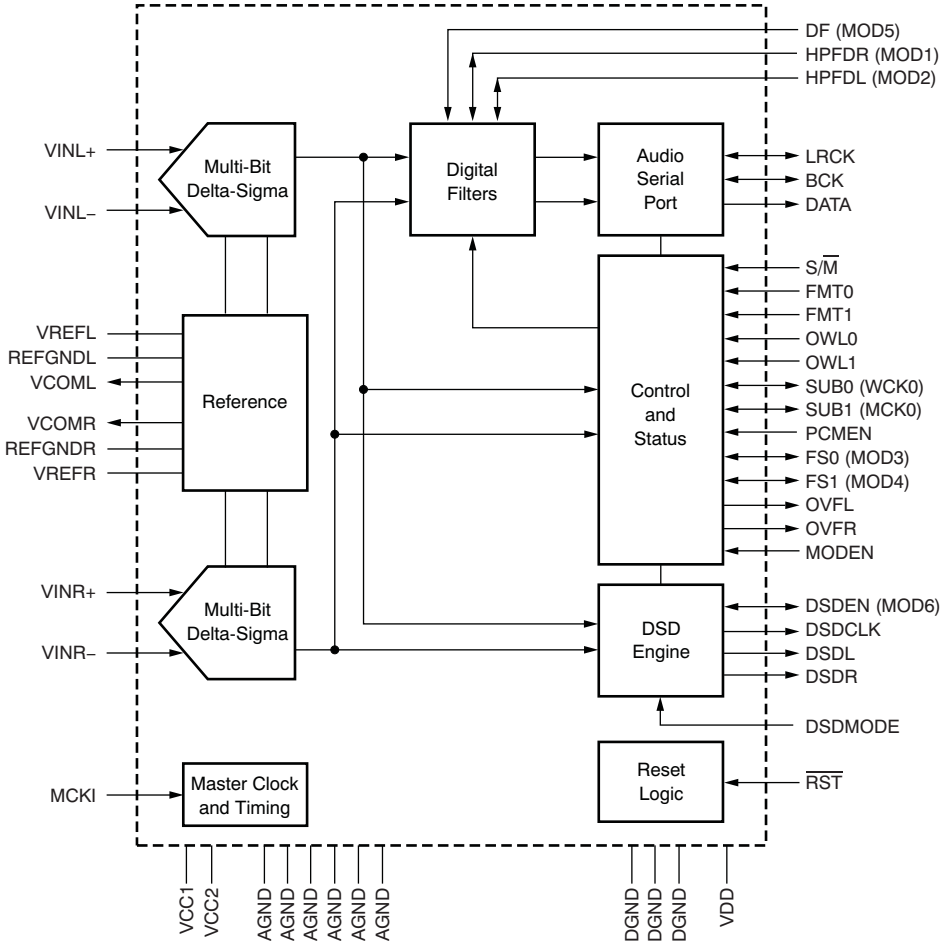

Figure 1. PCM4222 Functional Block Diagram

The primary features of the PCM4222EVM include:

- Simple configuration using switches and power-supply jumpers.
- Two differential input buffer/filter circuits employing the Texas Instruments OPA1632 fully differential amplifer integrated circuit.
- Two Texas Instruments DIT4192 digital audio interface transmitters, providing AES3-encoded output data. Transformer coupled 110Ω balanced and 75Ω unbalanced outputs are provided. Single-Channel, Double Sampling Frequency operation is supported.
- A buffered audio serial port header supports connection to external hardware or test equipment supporting Philips' I²S™, Left Justified, or Time Division Multiplexed (TDM) audio interface formats for PCM output data.
- A buffered data port header provides one-bit Direct Stream Digital (DSD) output data and the associated bit clock for the DSD output.
- A buffered modulator output port header provides access to the PCM4222 6-bit modulator data outputs and clocks.
- Support for onboard or external clock generation. Two onboard crystal oscillators provide support for common audio sampling rates, including 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, and 192kHz.
- Light emitting diode (LED) overflow indicators for the left and right audio channels.
- Minimum power-supply requirements: ±6V to ±15V for the analog section, and +5V for the digital section.
- The PCM4222 analog supply may be generated from an onboard +4.0 linear voltage regulator, or an external regulated dc power source.
- A +3.3V supply, used to power the majority of the digital circuitry and the PCM4222 digital section, may be generated from the +5.0V digital supply using an onboard linear voltage regulator. Alternatively, an external regulated dc power source may be selected, supporting digital supply voltages as low as +2.4V.

Figure 2 shows a simplified block diagram for the PCM4222EVM circuit functions. The blocks labeled *FDA* are the OPA1632 fully differential amplifier input circuits (U4 and U5). The blocks labeled *DIT* are the DIT4192 digital audio interface transmitters (U13 and U14). Two transmitters are required to support AES3 Single-Channel, Double Sampling Frequency applications.

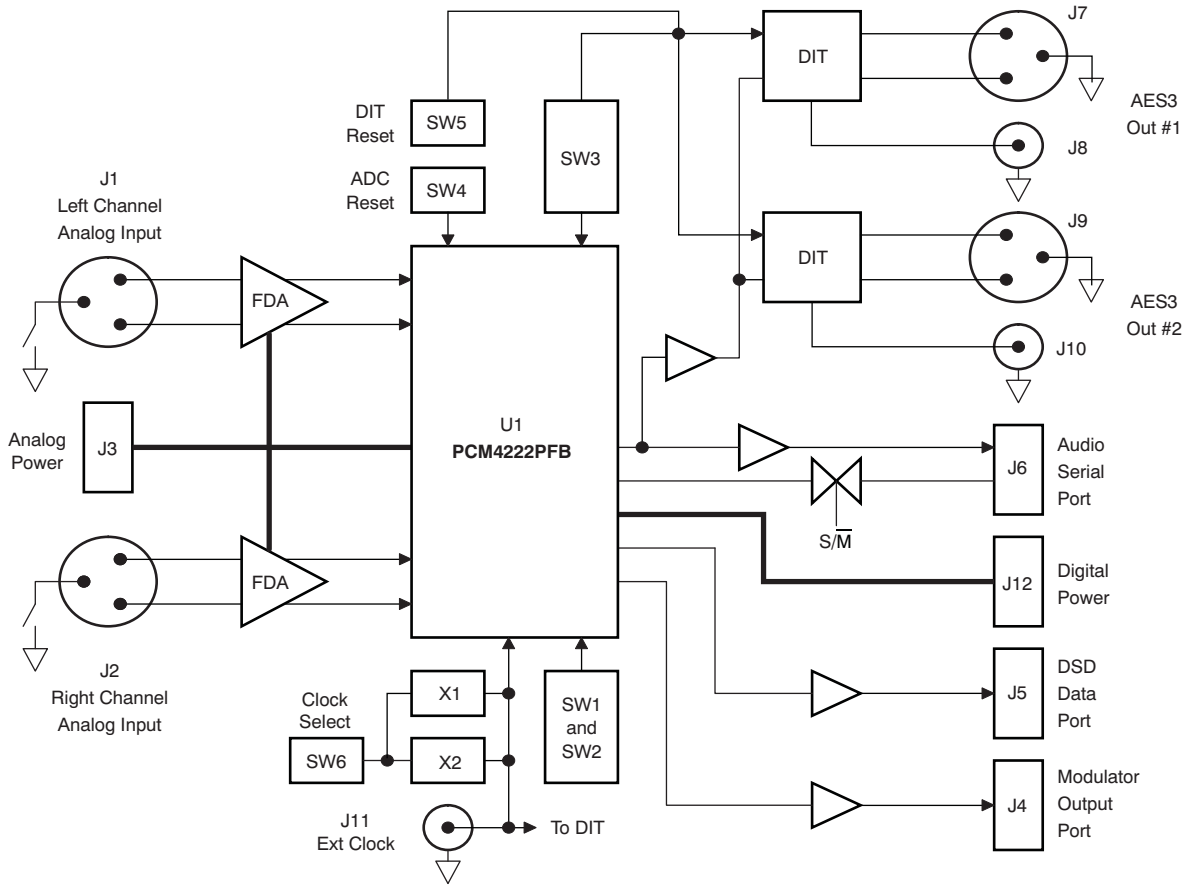

Figure 2. Simplified Block Diagram for the PCM4222EVM Evaluation Module

2 Hardware Configuration

This section provides information on the PCM4222EVM hardware configuration, including power supplies and switch settings. Evaluation module handling information and absolute operating conditions are also provided.

2.1 Electrostatic Discharge Warning

CAUTION

Failure to observe proper ESD handling procedures may result in damage to PCM4222EVM components.

Many of the components used in the assembly of the evaluation module are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling procedure when unpacking and handling the EVM. All handling should be performed at an approved ESD workstation or test bench while wearing an appropriate grounding device. Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Absolute Operating Conditions

CAUTION

Exceeding the absolute operating conditions may result in improper operation or damage to the evaluation module and/or the equipment connected to it.

Table 1 summarizes the critical data points for the PCM4222EVM absolute operating conditions.

Table 1. Absolute Operating Conditions

PARAMETER	MIN	MAX	UNIT
Analog Power Supplies			
+15V	-0.3	+16.0	VDC
-15V	+0.3	-16.0	VDC
EXT VCC	-0.3	+6.0	VDC
Digital Power Supplies			
+5V	-0.3	+5.5	VDC
EXT VDD	-0.3	+4.0	VDC
Analog Input Voltage (Measured Differentially at J1 or J2)			
Left Channel Analog Input (J1)		4 x VCC	$V_{PP\ (DIFF)}$
Right Channel Analog Input (J2)		4 x VCC	$V_{PP\ (DIFF)}$
Digital Input Voltage			
Audio Serial Port (J6)	-0.3	+4.0	V
EXT CLOCK (J11)	-0.3	+6.5	V
Digital Output Voltage			
Connectors J4, J5, and J6	-0.3	VDD + 0.3	
Connector J7, J9 (terminated with 110 ohms)		4.5	$V_{PP\ (DIFF)}$
Connector J8, J10 (terminated with 75 ohms)		3.6	V_{PP}
Temperature			
Ambient Operating Range	0	+70	°C

2.3 Power Supplies

The PCM4222EVM includes two terminal blocks for connection of external power supplies. Terminal block J3 supports analog power supplies, while terminal block J12 supports digital power supplies. Refer to Table 1 for absolute operating conditions. Table 2 shows the recommended power supply range for the PCM4222EVM.

Table 2. Recommended Power Supply Range

PARAMETER	MIN	MAX	UNIT
Analog Power Supplies (J3)			
+15V	+6.0	+15.0	VDC
-15V	-6.0	-15	VDC
EXT VCC	+3.8	+4.2	VDC
Digital Power Supplies (J12)			
+5V	+4.5	+5.5	VDC
EXT VDD	+2.4	+3.6	VDC

The PCM4222EVM requires a minimum of two external dc power supplies for the analog functions. The two power supplies are labeled as +15V and –15V on terminal block J3. The +15V and –15V supplies should be regulated and capable of providing a minimum of 200mA of current each.

The PCM4222 requires a +4.0V nominal dc supply for operation of the internal analog circuitry. Designated as VCC, this supply may be derived from the +15V analog power supply using an onboard linear regulator circuit, comprised of U23 and the associated components. The regulator circuit is protected in the event that a short-circuit occurs between the +15V supply and ground. The EVM also supports an external +4.0V power supply, which may be connected at the EXT VCC terminal of J3. Jumper JMP6 is used to select the onboard regulated supply or an external power source. Figure 3 illustrates the jumper options.

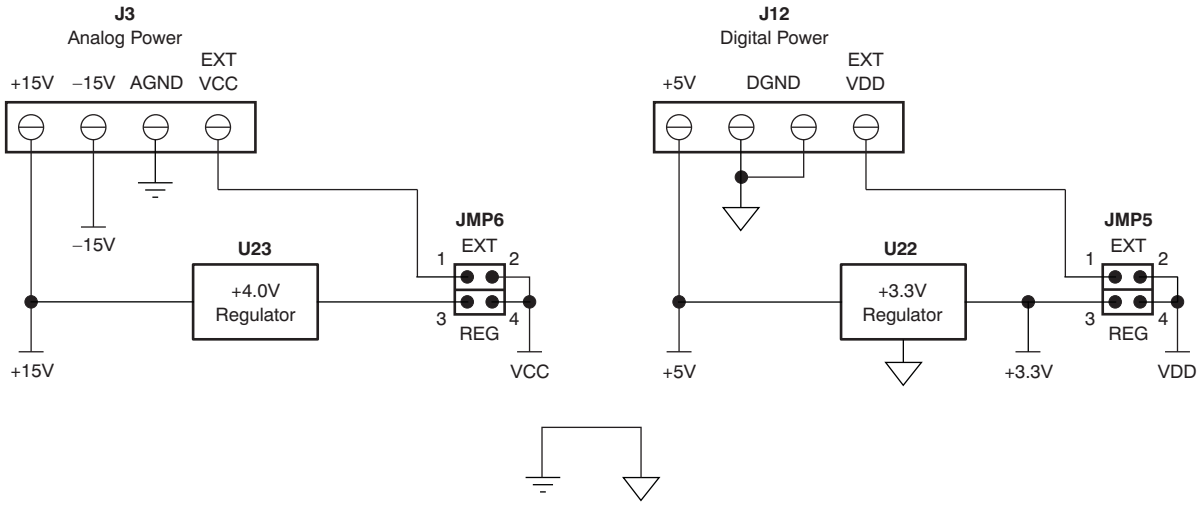

Figure 3. Power Supply Jumper Configuration

In addition to the analog supplies, the PCM4222EVM requires at least one digital power supply, connected at the +5V terminal of J12. This supply is nominally +5V dc, and should be provided by a regulated voltage source capable of sourcing a minimum of 200mA. The +3.3V required for the PCM4222 digital section and external support logic may be derived from the +5V supply using an onboard linear voltage regulator (U22). Alternatively, an external regulated VDD supply may be connected via the EXT VDD terminal of J12. Refer to Figure 3 for the configuration of jumper JMP5, which is used to select the source of the VDD power supply.

2.4 Analog Inputs

The left and right channel analog input sources for the PCM4222 are provided through connectors J1 and J2, respectively. The J1 and J2 connectors accommodate both 3-pin balanced XLR and 1/4-inch balanced TRS input connections. Pin 1 for both connector J1 and J2 include a ground lift jumper.

Each analog input is buffered by an input circuit employing the OPA1632 fully differential audio amplifier, selected for its low noise and distortion, and fully-differential input-to-output architecture. The buffer circuit provides attenuation (nominal gain = 0.482, or –6.34dB) and low-pass antialiasing filter functions. The printed circuit board (PCB) layout supports limited board stuff options for experimentation. The full-scale input voltage for the input buffer circuit is approximately $4.2V_{RMS}$ (or +14.6845dBu) differential, given a nominal VCC supply of +4.0V for the PCM4222 and a source impedance of 40Ω. Due to the full-scale input voltage varying slightly from one PCM4222 device to another, the full-scale input swing should be calibrated for each EVM individually, adjusting the input voltage level until a 0dBFS output level is indicated.

The common-mode bias for each OPA1632 is provided by the corresponding VCOML or VCOMR outputs from the PCM4222. The VCOML and VCOMR outputs are buffered by OPA227 low-noise precision op amps, configured as voltage followers. A buffer is required because of the low input impedance of the OPA1632 V_{OCM} pin.

2.5 Master Clock Source

The PCM4222 and the DIT4192 transmitters require a master clock source for operation. The master clock can be generated using one of two crystal oscillators (designated as X1 or X2), or from an external clock source connected at the BNC input connector J11. The clock generated by the crystal oscillators or external source is used directly by the DIT4192 transmitters. However, this clock must be divided by two when used by the PCM4222. A D-type flip-flop (U21) performs this function.

Oscillator X1 is fixed at 22.5792MHz, and may provide the master clock for 44.1kHz and related sampling rates, including 88.2kHz and 176.4kHz. Oscillator X2 is fixed at 24.576MHz, and may provide the master clock for 48kHz and related sampling rates, including 96kHz and 192kHz.

An external clock source (EXT CLOCK), may be input at BNC connector J11 and is buffered by U19. The buffer includes a tri-state output, so that it may be disabled when one of the crystal oscillators is used as the master clock source. Buffer U19 is always operated from the +3.3V supply generated by voltage regulator U22, and is tolerant to +5V input logic levels. The maximum external master clock frequency is 27.648MHz.

Table 3 summarizes the master clock source selection using switch SW6. Note that the user should not enable oscillators X1 and X2 simultaneously, because it will result in output contention and improper operation. Table 4 lists the master clock rate requirements for commonly used digital audio sampling rates.

Table 3. Master Clock Source Selection

Switch SW6, EXTCLK	Switch SW6, X2	Switch SW6, X1	Master Clock Selection
LO	LO	LO	External Clock connected at BNC input J11
HI	LO	HI	Oscillator X1, 22.5792MHz ±50ppm
HI	HI	LO	Oscillator X2, 24.576MHz ±50ppm
HI	HI	HI	Not allowed due to oscillator output contention

Table 4. Master Clock Frequencies for Common Output Sampling and Data Rates

PCM4222 Output Mode	Output Rate	EVM Master Clock Rate (MHz)	PCM4222 MCKI Clock Rate (MHz)
PCM Normal	8kHz	4.096	2.048
	32kHz	16.384	8.192
	44.1kHz	22.5792	11.2896
	48kHz	24.576	12.288
PCM Double Speed	88.2kHz	22.5792	11.2896
	96kHz	24.576	12.288
PCM Quad Speed	176.4kHz	22.5792	11.2896
	192kHz	24.576	12.288
DSD, 64x Oversampling	2.8224MHz	22.5792	11.2896
DSD, 128x Oversampling	5.6448MHz	22.5792	11.2896
Multi-Bit Modulator	6.144MHz	24.576	12.288

2.6 Manual Reset Operation

The PCM4222EVM includes two momentary-contact, normally open, push-button switches that are used for manual reset functions. Switch SW4 can be used to reset the PCM4222, while switch SW5 can be used to reset the DIT4192 transmitters. In each case, simply press and then release the corresponding push-button switch to force an external reset for these devices.

2.7 PCM Output Mode Configuration

The PCM4222 outputs linear encoded PCM data at the audio serial port output, header J6, or via the DIT4192 AES3 transmitters. The PCM data is binary two's complement, with the most significant bit of the data transmitted first. The audio data word length may be 24, 20, 18, or 16 bits. Several audio formats are supported. See section Section 2.7.2 (Audio Serial Port) of this document and the PCM4222 datasheet for details.

The PCMEN input (pin 16) is used to enable and disable the PCM output mode. Table 5 summarizes the operation of the PCMEN element on switch SW1. When the PCM output is disabled, the DATA (pin 32) output is forced low. If the PCM4222 is set to Master mode, the BCK (pin 33) and LRCK (pin 34) clock outputs are also forced low when the PCM output is disabled.

Table 5. PCM Output Mode Configuration

Switch SW1, PCMEN	PCM Output Mode
LO	PCM Output Disabled
HI	PCM Output Enabled

2.7.1 Sampling Mode

The PCM output operates in one three sampling modes: Normal, Double Speed, or Quad Speed. Normal mode supports 128x oversampling with output sampling rates up to 54kHz. Double Speed mode supports 64x oversampling with output sampling rates from 54kHz to 108kHz. Quad Speed mode supports 32x oversampling with output sampling rates from 108kHz to 216kHz.

The sampling mode is determined by the state of the FS0 and FS1 inputs (pins 19 and 20, respectively). FS0 and FS1 are configured using the like named elements of switch SW1. Table 6 summarizes the available settings for FS0 and FS1.

Table 6. PCM Sampling Mode Selection

Switch SW1, FS1	Switch SW1, FS0	PCM Sampling Mode
LO	LO	Normal
LO	HI	Double Speed
HI	LO	Quad Speed
HI	HI	Reserved

2.7.2 Audio Serial Port

For PCM mode, the audio data may be output via the audio serial port, which is buffered and routed to header J6. The audio serial port header pin configuration is shown in Table 7. The BCK and LRCK clocks may be outputs or inputs, depending upon the Master or Slave mode configuration of the port

Table 7. Audio Serial Port Header Configuration

Header J6 Pin Number	Audio Serial Port Signal Name, Description
1	SCKO, System Clock Output (same as PCM4222 MCKI clock)
3	BCK, Audio Data Bit Clock Input or Output
5	LRCK, Audio Left/Right Word Clock Input or Output
7	DATA, PCM Audio Data Output
2,4,6,8,9,10	Ground

In Master mode, the BCK and LRCK clocks are output pins, and are derived from the PCM4222 MCKI clock input (pin 35). The BCK clock rate depends on the audio data format selection. The LRCK clock rate is always equal to the output sampling rate. In Slave mode, the BCK and LRCK clocks are input pins, sourced from an external audio serial port master, such as a digital signal processor serial port, a serial timing generator, or a programmable logic device. Once again, the LRCK clock rate is always equal to the desired output sampling rate. The BCK clock rate depends on the audio data format selected. Refer to the PCM4222 datasheet for audio serial port operational details.

The Slave/Master mode operation is determined by the state of the S/$\overline{M}$ input (pin 39), which is controlled via the S/$\overline{M}$ element on switch SW3. Table 8 summarizes the operation of the S/$\overline{M}$ switch.

Table 8. Audio Serial Port Slave/Master Mode Selection

Switch SW3, S/$\overline{M}$	Slave or Master Mode
LO	Master
HI	Slave

The audio data format is selected using the FMT0 and FMT1 inputs (pins 44 and 43, respectively), which are controlled by the FMT0 and FMT1 elements on switch SW3. Table 9 summarizes the operation for the FMT0 and FMT1 switches.

Table 9. Audio Serial Port Data Format Selection

Switch SW3, FMT1	Switch SW3, FMT0	Audio Data Format
LO	LO	Left Justified
LO	HI	I^2S
HI	LO	TDM
HI	HI	TDM with One BCK Period Delay

When selecting a TDM data format, it is necessary to select a sub-frame assignment for the PCM4222 so that the device is set to transmit data during the appropriate time slots in the TDM frame. When the PCM4222 is not transmitting, the DATA output (pin 32) is forced to a high impedance state so that another PCM4222 device may transmit on the TDM data bus. The sub-frame assignment is selected using the SUB0 and SUB1 inputs (pins 26 and 25, respectively). These inputs are controlled using the SUB0 and SUB1 elements on switch SW2. Table 10 summarizes the operation for the SUB0 and SUB1 switches.

Table 10. TDM Sub-frame Assignment

Switch SW2, SUB1	Switch SW2, SUB0	Sub-Frame Assignment
LO	LO	Sub-Frame 0
LO	HI	Sub-Frame 1
HI	LO	Sub-Frame 2
HI	HI	Sub-Frame 3

Typically, the PCM4222 will be configured to output 24-bit PCM data. However, the PCM4222 supports data word length reduction using Triangular PDF dithering. This architecture allows the device to output 20, 18, or 16 bits of audio data when needed. The output word length is determined by the OWL0 and OWL1 inputs (pins 42 and 41, respectively). These pins are controlled by the OWL0 and OWL1 element switch SW3. Table 11 summarizes the operation of the OWL0 and OWL1 switches.

Table 11. PCM Output Word Length Selection

Switch SW3, OWL1	Switch SW3, OWL0	Output Data Word Length
LO	LO	24 bits
LO	HI	18 bits
HI	LO	20 bits
HI	HI	16 bits

2.7.3 Digital Decimation Filter

The PCM4222 includes a linear phase digital decimation filter that is used to downsample the delta-sigma modulator output and provide low-pass antialiasing filtering. The decimation filter includes two selectable frequency responses: Classic and Low Group Delay. Refer to the PCM4222 datasheet for plots and specifications related to each filter response. The DF input (pin 21) is used to select the desired frequency response. This input is controlled using the DF element on switch SW1. Table 12 summarizes the operation of the DF switch.

Table 12. Digital Decimation Filter Configuration

Switch SW1, DF	Digital Decimation Filter Response
LO	Classic
HI	Low Group Delay

2.7.4 Digital High-Pass Filter

The PCM4222 includes digital high-pass filtering that removes the dc component from the output signal. The right and left channel filters can be enabled and disabled individually, using the HPFDR (pin 17) and HPFDL (pin 18) inputs, respectively. These inputs are controlled via the HPFDR and HPFDL elements on switch SW1. Table 13 summarizes the operation for these switches.

Table 13. Digital High-Pass Filter Switch Operation

Switch SW1, HPFDR or HPFDL	Digital High-Pass Filter Function
LO	Enabled
HI	Disabled

2.7.5 Overflow Output Indicators

The PCM4222 includes two active-high overflow indicators, one each for the left and right channels. The overflow indicators are provided at the OVFL (pin 37) and OVFR (pin 38) outputs. These outputs are buffered by U17 and U18. The buffers drive light emitting diodes LED1 and LED2 on the EVM, providing visual overflow indication for the left and right channels, respectively.

2.7.6 AES3 Transmitter Operation

The EVM includes two Texas Instruments DIT4192 digital audio interface transmitters, U13 and U14. The transmitters accept either Left Justified or I^2S formatted PCM output data from the PCM4222 and then encode it into an AES3 data stream, which is output at connectors J7 through J10. A tri-state buffer (U11) is used to enable/disable the clock and data flow from the PCM4222 to the DIT4192 devices. The $\overline{\text{DIT}}$ switch on SW3 is used to enable or disable the buffer. Table 14 summarizes the $\overline{\text{DIT}}$ switch settings.

Table 14. DIT4192 Serial Data and Clock Enable Operation

Switch SW3, $\overline{\text{DIT}}$	DIT4192 Input Data/Clock Enable
LO	Enabled. Data and clocks flow from the PCM4222 to U13 and U14.
HI	Disabled. The tri-state buffer outputs are high impedance, with no clocks or data supplied to U13 and U14.

The DIT4192 includes an on-chip master clock divider, which is used to generate the output frame rate clock for the AES3-encoded data. For PCM data, the output frame rate is normally the same as the PCM4222 output sampling rate. The exception is for Single-Channel, Double Sampling Frequency transmission, when the DIT4192 Mono mode operation is invoked (this topic is discussed later in this section).

The DITCLK0 and DITCLK1 elements on switch SW3 determine the master clock divider settings for the transmitters. Table 15 summarizes the operation for the DITCLK0 and DITCLK1 switches, and indicates the selections corresponding to the three sampling modes for the PCM4222.

Table 15. DIT4192 Master Clock Divider Configuration

Switch SW3, DITCLK1	Switch SW3, DITCLK0	DIT4192 Master Clock Divider
LO	LO	Divide by 128 (PCM4222 Quad Speed mode)
LO	HI	Divide by 256 (PCM4222 Dual Speed mode)
HI	LO	Divide by 384 (Not Used)
HI	HI	Divide by 512 (PCM4222 Normal mode)

The DIT4192 input serial port supports Left Justified and I^2S formatted PCM data from the PCM4222 audio serial port. The TDM data formats are not supported by the DIT4192 input serial port. The DITFMT element on switch SW3 is used to select the proper data format for the DIT4192, and must match the data format that is selected using the FMT0 and FMT1 elements on switch SW3. Table 16 summarizes the operation for and relationship between the DIT4192 and PCM4222 data format switches.

Table 16. DIT4192 Data Format Selection

Switch SW3, FMT1	Switch SW3, FMT0	Switch SW3, DITFMT	Audio Data Format
LO	LO	LO	Left Justified
LO	HI	HI	I^2S
HI	X	X	TDM formats are not supported

Although one DIT4192 transmitter supports transmission of two-channels of PCM audio data at sampling/frame rates up to and including 216kHz, it is sometimes desirable to use two DIT4192 devices, each carrying data for only a single channel (left or right, respectively) at a frame rate equal to one-half the PCM4222 output sampling rate. This is referred to as Single-Channel, Double Sampling Frequency transmission in the AES3-2003 standard. The DIT4192 Mono mode is used to implement this form of transmission.

Mono mode is enabled or disabled using the MONO input (pin 21) of the DIT4192 transmitters. The DITMONO element on switch SW3 is used to control the MONO pin. Table 17 demonstrates the operation of the DITMONO switch.

Table 17. DIT4192 Transmission Mode Configuration

Switch SW3, DITMONO	DIT4192 Transmission Mode
LO	Two-channel
HI	Single-Channel Double Sampling Frequency

The MDAT input (pin 20) of the DIT4192 transmitters is used to select left or right channel for transmission in Mono mode. The MDAT pin of transmitter U13 is connected to ground, selecting the *left* input channel. The MDAT pin of transmitter U14 is connected to VDD, selecting the *right* input channel. In Mono mode, the *left* channel is transmitted from AES3 Output #1 (connectors J7 and J8), while the *right* channel is transmitted on AES3 Output #2 (connectors J9 and J10).

When Mono mode is disabled, both the left and right channels are output on both AES3 Output #1 and #2. This allows for simultaneous balanced and unbalanced transmission of the AES3-encoded output data.

Mono Mode Example: Assume that you are transmitting 192kHz two-channel data using the AES3 transmitters, with a 24.576MHz master clock and the clock dividers set to divide by 128. By simply enabling Mono mode (setting the DITMONO switch to HI), the transmission converts to Single-Channel, Double Sampling Frequency mode with an output frame rate equal to 96kHz. There is no need to change the master clock divider or frequency, because the DIT4192 manages the change in output frame rate automatically.

2.8 DSD Output Mode Configuration

The PCM4222 supports a one-bit Direct Stream Digital (DSD) data output, which operates at either 64x or 128x the base PCM output sampling rate. The PCM4222 allows both the DSD and PCM output modes to be enabled simultaneously. The DSD data for the left and right channels and the associated bit clock are output at the DSD data port, or header J5. Table 18 lists the pin configuration for header J5.

Table 18. DSD Data Port Header Pin Configuration

Header J5 Pin Number	DSD Data Port Signal Name, Description
1	DSDCLK, DSD Bit Clock Output
3	DSDL, One-bit DSD Data Output for the Left Channel
5	DSDR, One-bit DSD Data Output for the Right Channel
2,4,6,7,8,9,10	Ground

The DSD output mode is enabled or disabled using the DSDEN input (pin 22). This input is controlled via the DSDEN element on switch SW1. Table 19 summarizes the operation of this switch. When the DSD output is disabled, DSDCLK (pin 27), DSDL (pin 28), and DSDR (pin 29) are forced low.

Table 19. DSD Output Mode Configuration

Switch SW1, DSDEN	DSD Output Mode
LO	Disabled
HI	Enabled

The DSD output data rate may be set to 64x or 128x the base PCM rate (typically 44.1kHz). The output rate is selected via the DSDMODE input (pin 24). This input is controlled via the DSDMODE element on switch SW1. Table 20 summarizes the operation of this switch.

Table 20. DSD Output Rate Selection

Switch SW1, DSDMODE	DSD Output Data Rate
LO	64x Oversampled Data with Output Rate = MCKI ÷ 4
HI	128x Oversampled Data with Output Rate = MCKI ÷ 2

For more information regarding DSD output mode operation, timing, and specifications, see the PCM4222 datasheet.

2.9 Modulator Output Operations

The PCM4222 supports a multi-bit modulator (MBM) output mode, where the 6-bit data for the left and right channels are output directly from the delta-sigma modulators. The MBM output data are buffered and routed to the modulator data port, or header J4. Table 21 lists the pin configuration for header J4.

Table 21. Modulator Data Port Header Pin Configuration

Header J4 Pin Name	Modulator Data Port Signal Name, Description
1	MOD1, Modulator Data Output 1 (LSB)
3	MOD2, Modulator Data Output 2
5	MOD3, Modulator Data Output 3
7	MOD4, Modulator Data Output 4
9	MOD5, Modulator Data Output 5
11	MOD6, Modulator Data Output 6 (MSB)
13	MCKO, Modulator Data Clock Output (Rate = MCKI)
15	WCKO, Modulator Word Clock Output (Rate = MCKI ÷ 2)
2,4,6,8,10,12,14,16,17,18,19,20	Ground

The MBM output mode is enabled or disabled using the MODEN input (pin 23). This input is controlled via the MODEN element on switch SW1. Table 22 summarizes the operation of this switch. When MBM mode is enabled, the PCM and DSD output modes are disabled, because some of the pins used for these modes are remapped as modulator data and clock outputs. The PCMEN input (pin 16) must be set to the LO position when the MBM output is enabled. When MBM mode is disabled, all data and clock outputs associated with the interface are driven low (assumes PCM and DSD modes are also disabled).

Table 22. Multi-Bit Modulator (MBM) Output Mode Configuration

Switch SW1, MODEN	Switch SW1, PCMEN	Switch SW1, DSDEN	MBM Output Mode
LO	X	X	Disabled
HI	LO	X	Enabled

Referring to the electrical schematic in Figure 4, when MODEN is set to a LO state, the outputs of tri-state buffer U6 are enabled, allowing the elements of switch SW1 and SW2 that are related to the PCM and DSD output modes to control the configuration of the PCM4222. When MODEN is HI, the outputs of buffer U6 are disabled and set to a high-impedance state. In addition, when MODEN is HI, tri-state buffer U7 is enabled, allowing the modulator output data and clocks to be routed to the modulator data port (header J4).

For more information regarding Multi-Bit Modulator output mode operation, timing, and specifications, see the PCM4222 datasheet .

3 Hardware Reference

This section provides the electrical schematics and the Bill of Materials for the PCM4222EVM evaluation board. The components shown in the schematic are listed in Table 23, the Bill of Materials, for reference.

3.1 Electrical Schematics

The electrical schematics for the PCM4222EVM are shown in Figure 4 and Figure 5.

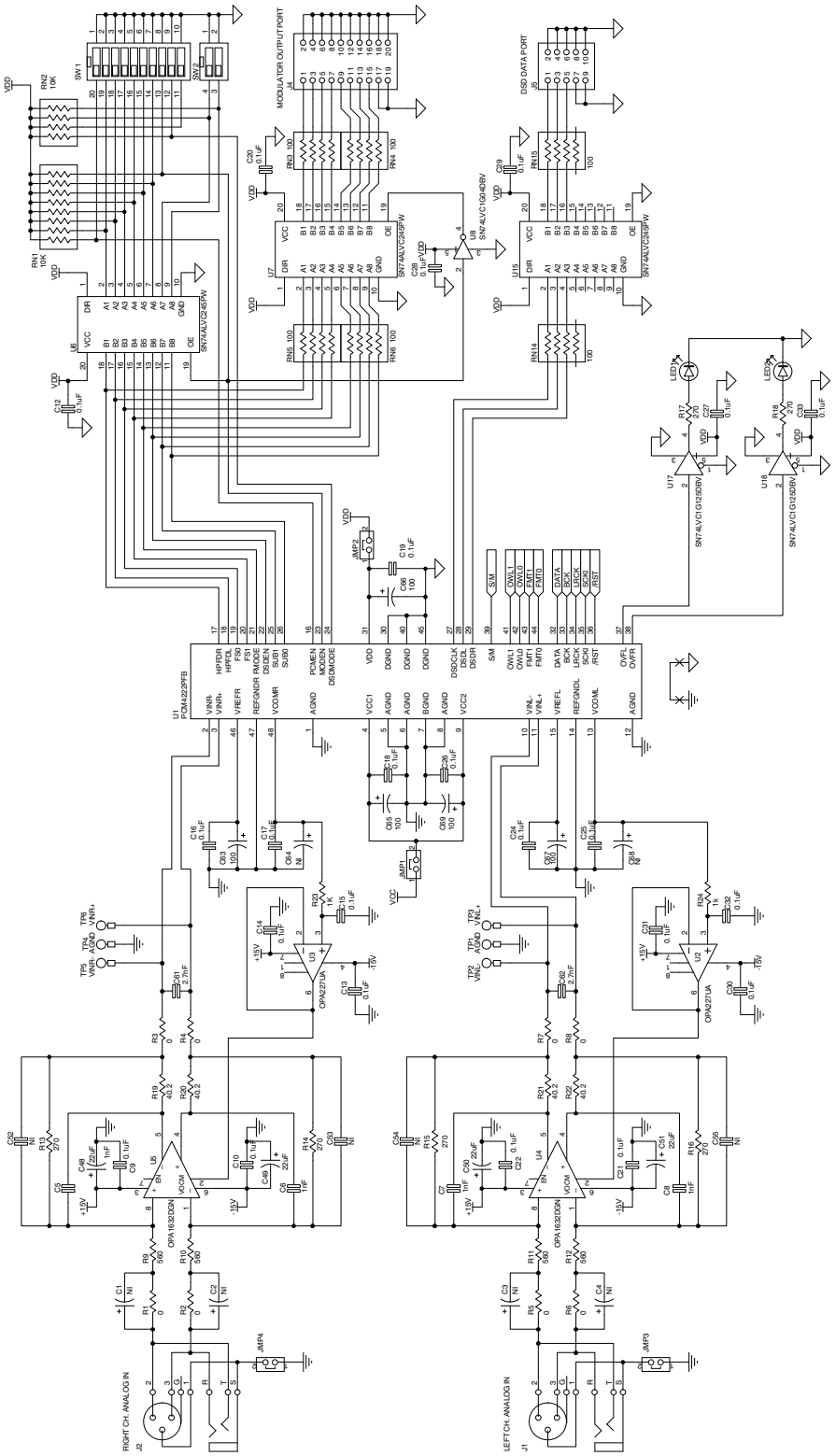

Figure 4. PCM4222EVM Schematics, Page 1 of 2

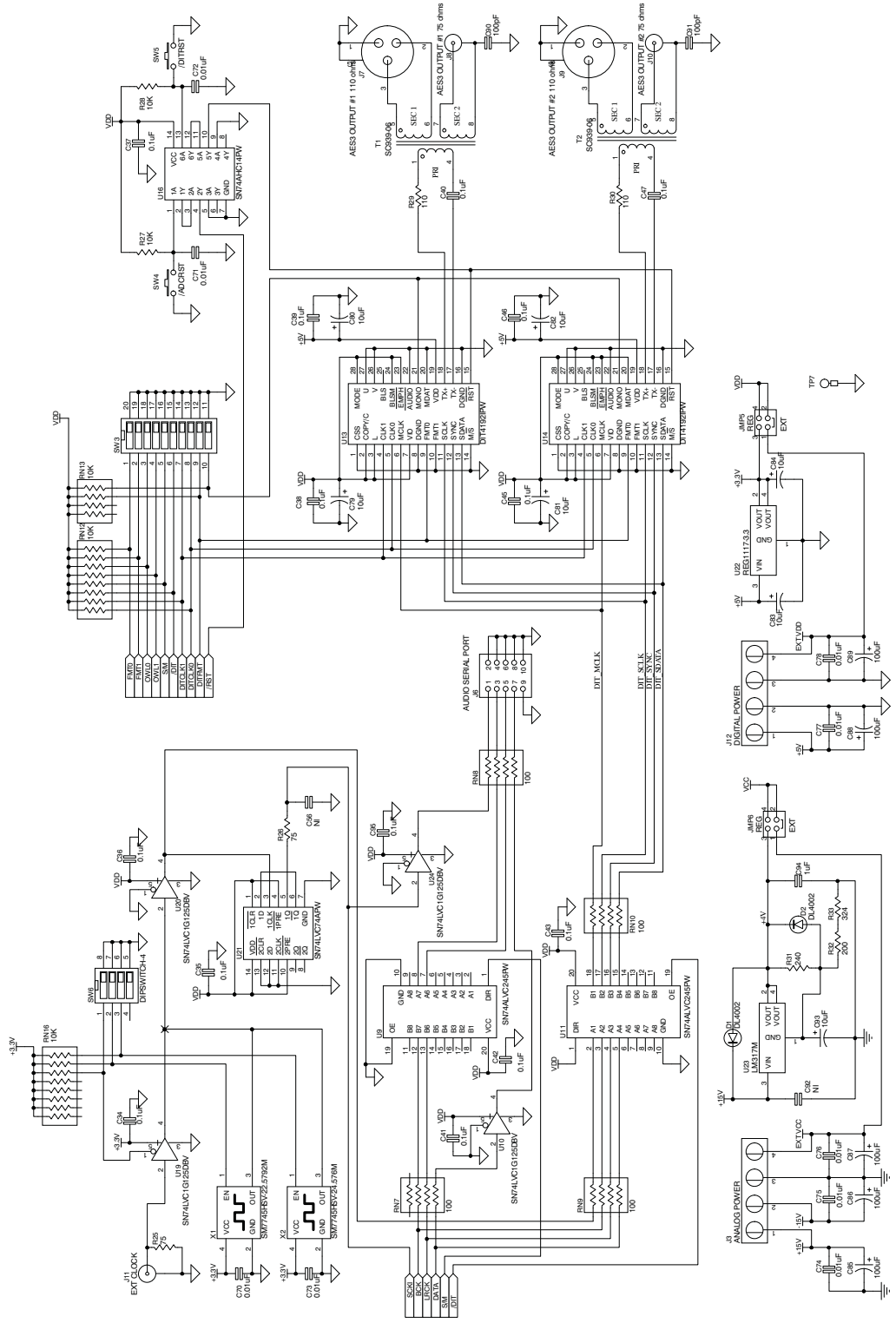

Figure 5. PCM4222EVM Schematics, Page 2 of 2

3.2 Bill of Materials

The Bill of Materials is provided as a cross-reference for the components shown in Figure 4 and Figure 5.

Table 23. Bill of Materials

ITEM	QTY	VALUE	REFERENCE DESIGNATOR	DESCRIPTION	VENDOR	PART NUMBER
1	NI		C1-C4	Optional AC Coupling Capacitor	N/A	N/A
2	2	100pF	C90, C91	Chip Capacitor, C0G Ceramic, 100pF ±5%, 50WV, Size = 0603	TDK	C1608C0G1H101
3	NI		C57-C60	Item Removed from Design	N/A	N/A
4	4	1nF	C5-C8	Chip Capacitor, PPS Film, 1nF ±2%, 50WV, Size = 0805 or Chip Capacitor, C0G Ceramic, 1nF ±5%, 50WV, Size = 0805	Panasonic or TDK	ECH-U1H102GX5 or C2012C0G1H102J
5	2	2.7nF	C61, C62	Chip Capacitor, PPS Film, 2.7nF ±2%, 50WV, Size = 0805 or Chip Capacitor, C0G Ceramic, 2.7nF ±5%, 50WV, Size = 0805	Panasonic or TDK	ECH-U1H272GX5 or C2012C0G272J
6	9	0.01µF	C70-C78	Chip Capacitor, X7R Ceramic, 0.01µF ±10%, 50WV, Size = 0603	TDK	C1608X7R1H103K
7	37	0.1µF	C9, C10, C12-22, C24-29, C30-C43, C45-C47, C95	Chip Capacitor, X7R Ceramic, 0.1µF ±10%, 50WV, Size = 0603	TDK	C1608X7R1H104K
8	NI		C92	Chip Capacitor, X7R Ceramic, 0.1µF ±10%, 50WV, Size = 0603	TDK	C1608X7R1H104K
9	1	1µF	C94	Chip Capacitor, X7R Ceramic, 1µF ±10%, 16WV, Size = 0603	TDK	C1608X7R1C105K
10	6	10µF	C79-C84	Chip Capacitor, Solid Tantalum, 10µF ±10%, 10WV, Size = A	Kemet	T491A106K010AT
11	1	10µF	C93	Chip Capacitor, Low ESR Tantalum, 10µF ±10%, 16WV, Size = B	Kemet	T494B106K016AT
12	NI	22µF	C48-C51	Chip Capacitor, Solid Tantalum, 22µF ±10%, 25WV, Size = D	Kemet	T491D226K025AT
13	5	100µF	C63, C65-C67, C69	Chip Capacitor, Polymer Tantalum, 100µF ±20%, 6.3WV, Size = B	Kemet	T520B107M006ATE070
14	NI	100µF	C64, C68	Chip Capacitor, Polymer Tantalum, 100µF ±20%, 6.3WV, Size = B	Kemet	T520B107M006ATE070
15	NI		C11, C23	Item Removed from Design	N/A	N/A
16	5	100µF	C85-C89	Capacitor, Alum Electrolytic, SMT, 100µF ±20%, 25WV	Panasonic	EEV-FK1E101XP
17	2		D1, D2	Rectifier, Passivated, 1A, 100V, SMD MELF	Micro Commerical Components	DL4002-TP
18	2		LED1, LED2	LED, SMT, Red Clear, Size = 1206	Lumex	SML-LX1206IC-TR
19	2		J1, J2	Combo Connector, Female XLR and TRS, Vertical PC Mount	Neutrik	NCJ6FI-H
20	2		J3, J12	3.5mm PCB Terminal Block, 4 poles	Weidmuller	996770
21	1		J4	Terminal Strip, 20-Pin (10x2)	Samtec	TSW-110-07-T-D
22	2		J5, J6	Terminal Strip, 10-Pin (5x2)	Samtec	TSW-105-07-T-D
23	2		J7, J9	3-Pin Male XLR Chassis Connector,Horizontal PC Mount	Neutrik	NC3MAH-0
24	2		J8, J10	RCA Phono Jack, Black Shell	CUI Stack	RCJ-041
25	1		J11	Vertical PCB Mount BNC Connector	Tyco/AMP	5414305-1
26	4		JMP1, JMP2, JMP3, JMP4	Terminal Strip, 2 pin (2x1)	Samtec	TSW-102-07-T-S
27	2		JMP5, JMP6	Terminal Strip, 4 pin (2x2)	Samtec	TSW-102-07-T-D
28	8	0Ω	R1-R8	Chip Resistor, 0Ω Shunt, Size = 0805	Panasonic	ERJ-6EY0R00V
29	4	40.2Ω	R19-R22	Chip Resistor, Thick Film, 1% Tolerance, 40.2Ω, 1/4W, Size = 1210	Panasonic	ERJ-14NF40R2U

Table 23. Bill of Materials (continued)

ITEM	QTY	VALUE	REFERENCE DESIGNATOR	DESCRIPTION	VENDOR	PART NUMBER
30	NI	75Ω	R25	Chip Resistor, Thick Film, 1% Tolerance, 75Ω, 1/10W, Size = 0805	Panasonic	ERJ-6ENF75R0V
31	1	75Ω	R26	Chip Resistor, Thick Film, 1% Tolerance, 75Ω, 1/10W, Size = 0805	Panasonic	ERJ-6ENF75R0V
32	2	110Ω	R29, R30	Chip Resistor, Thick Film, 1% Tolerance, 110Ω, 1/10W, Size = 0805	Panasonic	ERJ-6ENF1100V
33	1	200Ω	R32	Chip Resistor, Thin Film, 0.1% Tolerance, 200Ω, 1/10W, Size = 0805	Susumu or Digi-Key	RR1220P-201-B-T5 or RR12P200BCT-ND
34	1	240Ω	R31	Chip Resistor, Thin Film, 0.1% Tolerance, 240Ω, 1/10W, Size = 0805	Susumu or Digi-Key	RR1220P-241-B-T5 or RR12P240BCT-ND
35	6	270Ω	R13-R18	Chip Resistor, Metal Film, 0.1% Tolerance, 270Ω, 1/10W, Size = 0805	Panasonic	ERA-6YEB271V
36	1	324Ω	R33	Chip Resistor, Thin Film, 0.1% Tolerance, 324Ω, 1/10W, Size = 0805	Susumu or Digi-Key	RR1220P-3240-B-M-T5 or RR12P324BCT-ND
37	4	560	R9-R12	Chip Resistor, Metal Film, 0.1% Tolerance, 560Ω, 1/10W, Size = 0805	Panasonic	ERA-6YEB561V
38	2	1k	R23, R24	Chip Resistor, Thick Film, 1% Tolerance, 1kΩ, 1/10W, Size = 0805	Panasonic	ERJ-6ENF1001V
39	2	10k	R27, R28	Chip Resistor, Thick Film, 1% Tolerance, 10kΩ, 1/10W, Size = 0805	Panasonic	ERJ-6ENF1002V
40	10	100	RN3-RN10, RN14, RN15	Thick Film Chip Resistor Array 100Ω, 8 Terminal, 4 Resistors	CTS	742C083101JP
41	5	10k	RN1, RN2, RN12, RN13, RN16	Thick Film Chip Resistor Array 10kΩ, 16 Terminal, 8 Resistors	CTS	742C163103JP
42	NI		RN11, RN14, RN15	Item Removed from Design	N/A	N/A
43	2		SW1, SW3	DIP Switch, 10 Element, Half Pitch Surface-Mount, Tape Sealed	ITT C&K Switch	TDA10H0SB1
44	1		SW2	DIP Switch, 2 Element, Half Pitch Surface-Mount, Tape Sealed	ITT C&K Switch	TDA02H0SB1
45	2		SW4, SW5	Momentary Tact Switch SMT w/o Ground Terminal	Omron	B3S-1000
46	1		SW6	DIP Switch, 4 Element, Half Pitch Surface-Mount, Tape Sealed	ITT Cannon (formerly C&K)	TDA04H0SB1
47	2		T1, T2	Dual Zo Digital Audio Transformer	Scientific Conversion	SC939-06LF
48	7		TP1-TP7	PCB Test Point, Compact, Through-Hole	Keystone Electronics	5006
49	1		U1	High-Performance, 24-Bit/216kHz Stereo Audio A/D Converter	Texas Instruments	PCM4222PFB
50	2		U2, U3	Low-Noise Precision Op Amp	Texas Instruments or Texas Instruments	OPA227UAG4 or OPA27GU
51	2		U4, U5	Fully-Differential Audio Amplifier	Texas Instruments	OPA1632DGNG4
52	5		U6, U7, U9, U11, U15	Octal Bus Transceiver w/ Tri-State Output	Texas Instruments	SN74ALVC245PWG4 or SN74ALVC245PWRG4
53	1		U8	Single Inverter	Texas Instruments	SN74LVC1G04DBVRG4
54	6		U10, U17-U20, U24	Single Buffer w/ Tri-State Output	Texas Instruments	SN74LVC1G125DBVRG4
55	NI		U12	Item Removed from Design	N/A	N/A
56	2		U13, U14	Digital Audio Interface Transmitter	Texas Instruments	DIT4192IPWRG4
57	1		U16	Hex Schmitt Trigger Inverter	Texas Instruments	SN74AHC14PWG4 or SN74AHC14PWRG4
58	1		U21	Dual Positive Edge Triggered D-Type Flip-Flops with Clear and Preset	Texas Instruments	SN74LVC74APWRG4

Table 23. Bill of Materials (continued)

ITEM	QTY	VALUE	REFERENCE DESIGNATOR	DESCRIPTION	VENDOR	PART NUMBER
59	1		U22	Low Drop-Out Voltage Regulator, +3.3V	Texas Instruments or Texas Instruments or National Semiconductor or ON Semiconductor or Linear Technology	TLV1117-33CDCYG3 or TLV1117-33IDCYG3 or LM1117MP-3.3 or NCP1117ST33T3G or LT1117CST-3.3#PBF
60	1		U23	Linear Voltage Regulator, Adjustable	Texas Instruments or ON Semiconductor or National Semiconductor	LM317MDCYG3 or LM317MSTT3G or LM317EMP
61	1		X1	+3.3V, Surface-Mount Clock Oscillator, CMOS Output with Active High Enable, 22.5792MHz, ±50ppm	Pletronics	SM7745HSV-22.5792M
62	1		X2	+3.3V, Surface-Mount Clock Oscillator, CMOS Output with Active High Enable, 24.576MHz, ±50ppm	Pletronics	SM7745HSV-24.576M
63	6			Shorting Blocks	Samtec	SNT-100-BK-T-H
64	4			Self-Adhesive Rubber Feet	3M Bumpon	SJ-5003
65	1		PWB	PCM4222EVM PWB	Texas Instruments	6469498
66	NI		C52-C56	Stuff Option Capacitors, Size = 0805	N/A	N/A

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